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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Paper No. 18

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Appellant(s): Michio Asahina

Jay M. Finkelstein
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed 7/19/90.

(1) *Status of claims.*

The statement of the status of claims contained in the brief is correct.

This appeal involves claims 1-22.

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(3) *Summary of invention.*

The summary of invention contained in the brief is correct.

(4) *Issues.*

The appellant's statement of the issues in the brief is correct.

(5) *Grouping of claims.*

The rejection of claims 1-22 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together. See 37 C.F.R. § 1.192(c)(5).

(6) *Claims appealed.*

The copy of the appealed claims contained in the Appendix to the brief is correct.

(7) *Prior Art of record.*

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

4,672,419	McDavid	6-1987
4,593,454	Baudrant et al	6-1986
4,761,677	Sasaki	8-1988
4,725,877	Brasen et al	2-1988
IBM Technical Disclosure Bulletin, Vol. 21 No. 12	Howard	5-1979

(8) *New prior art.*

No new prior art has been applied in this examiner's answer.

(9) *Grounds of rejection.*

The following ground(s) of rejection are applicable to the appealed claims.

Claims 1-10,20 are rejected under 35 U.S.C. § 103 as being unpatentable over McDavid in view of Howard.

McDavid discloses a metal gate, interconnect and contact system for VSLI devices in Fig. 1. It comprises:

(a) a gate wiring [11];

(b) a substrate [10] having a doped semiconductor regions [26,27,25];

(c) a lower conductor structure [30];

(d) an insulating layer [31] overlying the lower conductor structure [30] and it has at least one opening extend to the lower conductor structure [30];

(e) an upper structure comprises a W layer [20], a Mo layer [21], a W layer [22] and Au layer [23] formed on the lower conductor structure [30] respectively.

Howard discloses a conductor structure in fig. 2. It comprises"

(a) a Si substrate;

(b) a lower conductor structure [3] made of transition metal nitride can be produced by reacting evaporation, reactive sputtering in Ar:Nz atmosphere, or sputtering of a preformed target of the nitride;

(c) an Al-Cu or Au upper conductor structure formed on the lower conductor structure [3];

(d) a metal nitride layer [2] made from the same process as the conductor structure [3] formed on the Al-Cu or Au upper conductor structure;

(e) a 2nd Al-Cu or Au layer formed on the metal nitride layer [2].

Since both McDavid and Howard has an interconnect and contact system for silicon semiconductor device, it would have

been obvious to have the conductor structure of Howard in McDavid because it is able to improve the electromigration resistance of the wiring structure and it is able to avoid the formation of cracks.

Claim 11 is rejected under 35 U.S.C. § 103 as being unpatentable over McDavid in view of Howard, further in view of Baudrant et al.

McDavid discloses a semiconductor region of an impurity doped polycrystalline Si. Baudrant discloses a semiconductor regions [10,16] in fig. 7 comprises of monocrystalline or polycrystalline Si.

Since both McDavid and Baudrant et al are insulated gate FET device, it would have been obvious to one of the ordinary skill in the art to have the monocrystalline Si material of Baudrant et al in McDavid because it is a common semiconductor material.

Claims 12,13,15,16 and 17 are rejected under 35 U.S.C. § 103 as being unpatentable over McDavid in view of Howard, further in view of Sasaki.

Sasaki discloses a semiconductor device having a conductive interconnection structure in fig. 5. It comprises a Si substrate [1] with source and drain regions and an insulated gate formed between them. A lower conductive polyacetylene layer [20b] contacts with the source and drain region. An upper conductor portion [21] is made of Al connects to the lower conductive portion through the insulating layer [20a]. An insulating layer [22a] having an opening overlying the upper conductive structure

[21] and insulating layer [20a] and a conductive polyacetylene layer [22b] formed within the opening. An Al layer [23] connected to the conductive layer [22b].

Since both McDavid and Sasaki have a conductive layer formed on the upper conductive layer through an opening, it would have been obvious to one of the ordinary skill in the art to have the metal layer that contact with the upper conductive layer of McDavid formed only in the opening of the insulating layer in Sasaki because it is a common interconnecting wiring structure.

Claims 14,18 and 19 are rejected under 35 U.S.C. § 103 as being unpatentable over McDavid in view of Howard, Sasaki and Brasen et al.

Brasen et al discloses a metallized semiconductor device in the figure. It comprises a metal plating layer [13] deposits on the gate wiring [9], the metallized upper conductor structure [111,112,113] of the lower drain electrode [8] and the metallized upper conductor structure [10] of the lower source electrode [7].

Since both McDavid and Brasen et al have a metallized layer formed on the lower conductive layer, and within the opening of the insulating layer [12], it would have been obvious to one of the ordinary skill in the art to have the metallized layer of Brasen et al in McDavid because it is a common interconnecting wiring structure.

Claims 21 and 22 are rejected under 35 U.S.C. § 103 as being

unpatentable over Sasaki in view of Howard.

Sasaki discloses a semiconductor device having a conductive interconnection structure in fig. 2. It comprises a substrate [1] with source and drain region [S,D] and insulated gate [G]. A lower conductor portion is made of conductive polyacetylene layer [10a] and covered by an insulating layer [12a]. A conductive polyacetylene connected to the conducting layer [10a] through an opening in the insulating layer [12a] and a conductor structure [14b] connected to the conductor layer [12a].

Since both Sasaki and Howard have a conducting layer formed within the opening of the insulating layer, it would have been obvious to one of ordinary skill in the art to have the interconnection structure of Howard in Sasaki because it is a common interconnection wiring structure.

(10) *New ground of rejection.*

This Examiner's Answer does not contain any new ground of rejection.

(11) *Response to argument.*

In regard to Appellant's arguments on pages 4 and 6 of the Appeal Brief, it is true that the transition metal nitrides of Howard is not an electroplated or electrolessly plated layer. The metal nitrides of Howard is produced by reacting evaporation, reactive sputtering in Ar:Nz atmosphere, or sputtering of a preformed target of the nitride. However, it is important to

note that the process limitation of how the electrical conductor is formed has no patentable weight in claim drawn to structure. Note that:

A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not.

See also MPEP 706.03(e).

Such term as "electroplated", "electrolessly plated" in claims 1 and 21 and "electrolytically plated" in claim 5 are thus non-limiting.

Also, as in re Thorpe, 777 F.2d 695, 227 USPQ 964 (Fed. Cir. 1985):

The patentability of a product does not depend on its method of production. In re Pilkington, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969). If the product in a product by-process claim is the same as or obvious from a product of the

prior art, the claim is unpatentable even though the prior product was made by a different process. In re Marosi, 710 F.2d 799, 803, 218 USPQ 289, 292-93 (Fed. Cir. 1983); Johonson & Johnson V. W.L. Gore, 436 F. Supp. 704, 726, 195 USPQ 487, 506 (D. Del. 1977); see also In re Fessman, 489 F.2d 742, 180 USPQ 324 (CCPA 1974).

In addition, both the electroplated or electrolessly plated metal layer of the applicant and the sputtered layer or evaporated metal nitride layer of Howard would reduced the tendency to form voids in the underlying metallized layer. This shows the difference between the applicants invention and the prior art are just the process to produce an identical product. The physical structure of both devices are the same. It is also important to note the metallized conductor [20,21,22,23] can be produced by sputtering or CVD. which are well-known in the art of metallization of interconnect and ohmic contact system in semiconductor devices.

In regard to page 7 of the appeal brief, the rejection of claim 22 under 35 USC 112, 2nd paragraph is withdrawn and the rejection of claims 5-7,10 and 13 under USC 112, 4th paragraph (a mistake was being made in the final rejection, claim 5-7,10,13 are rejected under USC 112, 4th paragraph, accordingly to the 1st office action, not USC 112, 2nd paragraph) are also withdrawn.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Loke/rk
September 19, 1990

ROLF HILLE
SUPERVISORY PATENT EXAMINER
ART UNIT 258

Spensley Horn Jubas & Lubitz
STE 500
1880 Century Part East
Los Angeles, CA 90067